REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 1, 2, and 5-30 are pending. Claims 1, 2, and 5-30 stand rejected.

Claims 1, 15, and 23 have been amended. No claims have been canceled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

Applicants reserve all rights with respect to the applicability of the Doctrine of Equivalents.

CLAIMS OBJECTIONS

The Examiner has objected to Claim 10 for being identical to claim 9. Applicants respectfully disagree.

Claim 10 includes "connecting the resistive/capacitive network between a driver of an input/output circuit and a receiver of the input/output circuit."(emphasis added).

Claim 9, however, includes "connecting the resistive/capacitive network between a driver of a first input/output circuit and a receiver of a second input/output circuit." (emphasis added) Therefore, applicants respectfully submit that claim 10 is not identical to claim 9.

REJECTIONS UNDER 35 U.S.C. § 103

Claims 1-2, 5-11, 15-18, and 22-30 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,054,863 of Morrison et al. ("Morrison").

Amended claim 1 reads as follows:

A computer-implemented method comprising:

> measuring first electrical characteristics of an interconnection, including generating a first graphical representation of a first output of the interconnection that is based, at least in part, on the first electrical characteristics; and

determining a test network that emulates the interconnection, the test network having second electrical characteristics that includes determining resistive and capacitive values such that the measured first electrical characteristics of the interconnection are approximated by the resistive and capacitive values of the test network within a specified tolerance, wherein determining the resistive and capacitive values includes adjusting the resistive and capacitive values based on the first graphical representation, wherein the determining the test network includes creating a second graphical representation of a second output of the test network based on the adjusted resistive and capacitive values, wherein the second graphical representation approximates the first graphical representation of the first output of the interconnection within a specified tolerance.

(Amended claim 1)(emphasis added)

Morrison discloses a system for testing circuit board integrity. More specifically, Morrison discloses:

> …a system for testing circuit boards, comprising:
> ...a timing circuit having an output for outputting a pulse to the node having the address generated by the node address generator and coupling the remaining nodes to electrical ground…

(Morrison, col. 2, lines 49-59)(emphasis added)

In particular, Morrison discloses:

> Each timer circuit 24a-n has a trigger input 34a-n, discharge terminal 36a-n, external capacitor terminal 38a-n and output 40a-n, respectively. In a preferred embodiment, each timer-circuit is a CMOS type timer. Each discharge terminal and external capacitor terminal are coupled to a corresponding node. For example, discharge terminal 36a and external capacitor terminal 38a are coupled to Node 1. Each resistor 28a-n is coupled between the supply voltage V.sub.CC and a node. In a preferred embodiment, V.sub.CC is about 15 volts d.c. and each resistor has a resistance between about 100 K.OMEGA. and 2M.OMEGA. ohms. The actual resistance of each resistor 28a-n depends on the size of the circuit board being tested and the number of nodes and probes utilized in system 10. Each resistor 28a-n is coupled to NET1-N, respectively, through probes P.sub.1-N, respectively. The capacitance of each net C.sub.NET1-N and resistors 28a-n, respectively, form a plurality of R/C (resistor/capacitor) timing circuits. Since each discharge terminal 36a-n and external capacitor terminal 38a-n of each timer 24a-n, respectively is coupled to a Node 1-N, respectively, each R/C timing circuit becomes the R/C timing circuit for a corresponding timer circuit 24a. When each trigger input 34a-n of timer circuits 24a-n, respectively, receives a trigger signal 32a-n, respectively, a pulse 27 is outputted at output terminals 40a-n, respectively.

(Morrison, col. 5, lines 30-43)(emphasis added)

Morrison discloses:

> …a timing circuit having an output for outputting a pulse with a pulse width, and coupled to a resistor to form an R/C timing circuit with said network capacitance

to the node having the address generated by the node address generator and coupling the remaining nodes to electrical ground, …

(Morrison, col. 7, lines 59-64)(emphasis added)

Thus, Morrison merely discloses the timing circuit coupled to the resistor to form a R/C timing circuit. In contrast, amended claim 1 refers to measuring first electrical characteristics of an interconnection, including generating a first graphical representation of a first output of the interconnection that is based, at least in part, on the first electrical characteristics; and determining a test network that emulates the interconnection, the test network having second electrical characteristics that includes determining resistive and capacitive values such that the measured first electrical characteristics of the interconnection are approximated by the resistive and capacitive values of the test network within a specified tolerance, wherein determining the resistive and capacitive values includes adjusting the resistive and capacitive values based on the first graphical representation, wherein the determining the test network includes creating a second graphical representation of a second output of the test network based on the adjusted resistive and capacitive values, wherein the second graphical representation approximates the first graphical representation of the first output of the interconnection within a specified tolerance.

Therefore, applicants respectfully submit that claim 1 is not obvious under 35 U.S.C. § 103(a) over Morrison.

Given that claims 2, 5-11, 15-18, and 22-30 contain limitations that are similar to those discussed with respect to amended claim 1, applicants respectfully submit that claims 2, 5-11, 15-18, and 22-30 are not obvious under 35 U.S.C. § 103(a) over Morrison.

Claims 12-14, and 19-21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Morrison, and further in view of Neil H. E. Weste et al., "Principles of CMOS VLSI Design: A System Perspective", 2nd Edition, Addison-Wesley Publishing Company, 1993 ("Neil").

It is respectfully submitted that Morrison does not teach or suggest a combination with Neil, and Neil does not teach or suggest a combination with Morrison. It would be impermissible hindsight, based on applicants' own disclosure, to combine Morrison and Neil.

Morrison teaches the system for testing the circuit board integrity (Abstract).

Neil, in contrast, teaches principles of CMOS VLSI design (Abstract).

Furthermore, even if the CMOS VLSI design of Neil were incorporated into the system for testing the circuit board integrity of Morrison, such a combination would still lack to measuring first electrical characteristics of an interconnection, including generating a first graphical representation of a first output of the interconnection that is based, at least in part, on the first electrical characteristics; and determining a test network that emulates the interconnection, the test network having second electrical characteristics that includes determining resistive and capacitive values such that the measured first electrical characteristics of the interconnection are approximated by the resistive and capacitive values of the test network within a specified tolerance, wherein determining the resistive and capacitive values includes adjusting the resistive and capacitive values based on the first graphical representation, wherein the determining the test network includes creating a second graphical representation of a second output of the test network based on the adjusted resistive and capacitive values, wherein the second graphical representation approximates the first graphical representation of the first output of the interconnection within a specified tolerance, as recited in amended claim 1.

Given that claims 12-14, and 19-21 contain the limitations that are similar to those discussed with respect to amended claim 1, applicants respectfully submit that claims 12-14, and 19-21 are not obvious under 35 U.S.C. § 103(a).

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call the undersigned attorney at (408) 720-8300.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

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